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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,560	01/16/2001	Kenny Kok-Hoong Chiu	052404.0098	3810

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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,560	CHIU, KENNY KOK-HOONG	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,13-15,17-22,27-30 and 32-37* is/are rejected.

7)☒ Claim(s) *10-12,24-26 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-9, 13-15, 17-22, 27-30, 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt (US Patent 5,675,615) in view of Iknaian et al. (US Patent 5,294,842).

(1) With regard to claim 1, Watt discloses in Fig. 5, a clock selection device adapted to select one of a pair of clock sources onto an output clock line, comprising: a first input clock line (mclk) coupled to a first clock source; a second input clock line (fclk) coupled to a second clock source, the second clock source asynchronous to the first clock source (col. 5, lines 46-50); and a clock selection logic (28) adapted to select from the first input clock line and the second input clock line, producing an internal clock line coupled to the output clock line (col. 6, lines 47-63); and a clock synchronization logic (Synchroniser Cir) coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock

line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free (col. 4, lines 12-20).

Watt does not however teach wherein the clock synchronization logic is independent of the internal clock line.

However, Iknaian et al. teaches in Fig. 4, wherein the clock synchronization logic (78) is independent of the internal clock line (29).

One skilled in the art would have clearly recognized that clock synchronization logic independent of the internal clock line is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Iknaian et al. to modify the invention of Watt as a method of redistributing multiple copies of an updated, low-skew clock signals to circuitry on a module without disrupting the continuous flow of output clock signals (col. 2, lines 28-40).

(2) With regard to claim 2, Watt also discloses, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

(3) With regard to claim 4, Watt also discloses the clock selection device of claim 3, the clock synchronization logic comprising: a first clock synchronization block (Synchroniser Cir), coupled to the first clock source, adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block, coupled to the second clock source (Synchroniser Cir), adapted to synchronize the second clock source and the clock selection logic.

(4) With regard to claim 5, Watt also discloses the clock synchronization logic further comprising: a first clock reset signal (fNm), synchronized to the first clock signal, adapted to

reset the first clock synchronization block; and a second clock reset signal (reset), synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 7, lines 7-23).

(5) With regard to claim 6, Iknaian et al. also teaches the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 5, line 37- col. 6, line 28).

(6) With regard to claim 7, Iknaian et al. also teaches in Fig. 4, wherein the clock selection logic (77) comprises a multiplexer with two clock input lines (A_CLK, B_CLK).

(7) With regard to claim 8, Iknaian et al. also teaches wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level (col.2, line 67 – col. 3, line 10).

(8) With regard to claim 9, Iknaian et al. also teaches a clock selection signal, asynchronous to the first clock source and the second clock source (col. 2, lines 43-59), adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is selected (col. 7, lines 12-15).

(9) With regard to claim 13, Watt also discloses in Fig. 5, a buffer (24) coupled to the internal clock line, producing a buffered output clock signal.

(10) With regard to claim 14, as noted above, Watt in combination with Iknaian et al. disclose the clock selection device as disclosed in claim 1 and 14. Furthermore, Iknaian et al's

invention relates to synchronization of clock signals in a computer system. Therefore, a processor would be obvious as would be the use of the synchronization device throughout the computer system through a plurality of communication controllers to incorporate its benefits throughout the system. Watt also discloses in Fig. 1, the use of his invention in a processor based system.

(11) With regard to claim 15, Watt also discloses, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

(12) With regard to claim 17, Watt also discloses the clock selection device of claim 3, the clock synchronization logic comprising: a first clock synchronization block (Synchroniser Cir), coupled to the first clock source, adapted to synchronize the first clock source and the clock selection logic; and a second clock synchronization block, coupled to the second clock source (Synchroniser Cir), adapted to synchronize the second clock source and the clock selection logic.

(13) With regard to claim 18, Watt also discloses the clock synchronization logic further comprising: a first clock reset signal (fNm), synchronized to the first clock signal, adapted to reset the first clock synchronization block; and a second clock reset signal (reset), synchronized to the second clock signal, adapted to reset the second clock synchronization block, wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic (col. 7, lines 7-23).

(14) With regard to claim 19, Iknaian et al. also teaches the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic (col. 5, line 37- col. 6, line 28).

(15) With regard to claim 20, claim 20 inherits all limitations of claim 14. Furthermore, Iknaian et al. also teaches in Fig. 4, wherein the clock selection logic (77) comprises a multiplexer with two clock input lines (A_CLK, B_CLK).

(16) With regard to claim 21, claim 21 inherits all limitations of claim 20 above. Furthermore, Iknaian et al. also teaches wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level (col.2, line 67 – col. 3, line 10).

(17) With regard to claim 22, claim 22 inherits all limitations of claim 14, above. Furthermore, Iknaian et al. also teaches a clock selection signal, asynchronous to the first clock source and the second clock source (col. 2, lines 43-59), adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is selected (col. 7, lines 12-15).

(18) With regard to claim 27, Watt also discloses in Fig. 5, a buffer (24) coupled to the internal clock line, producing a buffered output clock signal on the output clock line.

(19) With regard to claim 28, claim 28 inherits all limitations of claim 1 above as claim 28 merely cites the method used by the clock selection device disclosed in claim 1.

(20) With regard to claim 29, claim 29 inherits all limitations of claim 28. Furthermore, Watt also discloses the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

(21) With regard to claim 30, Watt also discloses in Fig. 5, buffering (24) the internal clock line to generate the output clock line.

(22) With regard to claim 32, Watt also discloses the delaying step (c) for a predetermined amount of time (abstract).

(23) With regard to claim 33, Watt also discloses resetting a synchronization logic with a first reset signal synchronous to the first clock signal; and resetting the synchronization logic with a second reset signal synchronous to the second clock signal (col. 7, lines 7-23).

(24) With regard to claim 34, Watt also discloses the method of claim 28, step (c) comprising the steps of (cl) receiving a clock select signal asynchronous to the first clock signal and the second clock signal; and (c2) connecting the first clock signal to the output clock line when the clock select signal is asserted; (c3) connecting the second clock signal to the output clock line when the clock select signal is deasserted; (c4) synchronizing the first input clock signal, the second input clock signal, and steps (c2) and (c3), such that the output clock line is glitch free (col. 3, lines 14-42).

(25) With regard to claim 35, claim 35 inherits all limitations of claim 1 above. Watt discloses in Fig. 5, a clock switching mechanism with guaranteed stability a clock switching mechanism with guaranteed stability, comprising; a clock switching means (28) for switching a clock source of a first clock source (mclk) and a second clock source (fclk) to an output clock line, the second clock source asynchronous to the first clock source (col. 5, lines 46-50); and a clock synchronizing means (Synchronizer clr) coupled to the first and the second clock sources and the clock switching means, the clock synchronization means guaranteeing the output clock line is glitch free (col. 4, lines 12-20) and Iknaian teaches in Fig. 4, the clock synchronization means is independent of the output clock line.

(26) With regard to claim 36, Watt also discloses in Fig. 5, the clock synchronization logic further comprising: a first reset means (36) synchronized to the first clock source for resetting the clock synchronization means; and a second means (reset), synchronized to the second clock source for resetting the clock synchronization means, wherein the first reset means and the second reset means signal can prevent meta-stability of the clock synchronization means (col. 7, lines 7-23).

(27) With regard to claim 37, Watt also discloses the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency (abstract).

Allowable Subject Matter

4. Claims 10-12, 24-26 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 703-305-6969. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
October 14, 2004

Amanda Le

AMANDA T. LE
PRIMARY EXAMINER